

# Silicon Metal-Insulator-Semiconductor Field-Effect Transistor Prototypes for SrTiO<sub>3</sub> MISFET Fabrication

by Colin Drummond and Dan McKeon 2005

## Abstract

This paper details an attempt to fabricate a metal-insulator-semiconductor field-effect transistor (MISFET), using a strontium titanate (SrTiO<sub>3</sub>) substrate. The MISFET for our project was designed to induce a change in the superconducting temperature of the transistor, made possible since doped super-cooled SrTiO<sub>3</sub> acquires the property of superconductivity. This effect creates a potentially valuable component in microelectronic fabrication of superconducting devices.

We first fabricated a MISFET prototype using a silicon substrate. We were unable to characterize the electrical capabilities of our first prototype because of problems with sonication. Since sonication dislodged gold from the substrate, we altered our procedure so that we only sonicated before sputtering and then stored the substrate between depositions to keep it clean. The second difficulty we encountered was a faulty QCM crystal, which we were able to replace.

On our SrTiO<sub>3</sub> substrate MISFET prototype, we made changes to our procedure. We changed the way we loaded the masks and we substituted aluminum for the point contacts in the second prototype (in the first prototype we used gold), because there was lower resistivity between aluminum and SrTiO<sub>3</sub> than there was between gold and SrTiO<sub>3</sub>. Due to the fragility of the SrTiO<sub>3</sub> substrate, we had to elevate the mask above it, which caused problems when evaporating aluminum onto the substrate. We increased the radius of the coil to match the radius of the aluminum wire, but since the tungsten could not be coiled tightly enough the aluminum melted out of the coil.

## Introduction

This paper details an attempt to fabricate a metal-insulator-semiconductor field-effect transistor (MISFET), using a strontium titanate (SrTiO<sub>3</sub>) substrate. (For terms, see Glossary in Appendix.) In its doped form, SrTiO<sub>3</sub> exhibits the properties of a superconductor and is a potentially valuable substrate material. As a substrate, SrTiO allows for easy growth of manganites and cuprates, which are used in microelectronic switching applications such as transistors and microchips (1). Today, transistors are the dominant solid-state devices in the world (2). They are substantially smaller than the first transistors and millions exist in such devices as cell phones and computers (3).

The key components of a MISFET are the substrate, a source, a drain, a gate, and an insulator. The substrate is the main part of the transistor, and the traditional material used as a substrate is silicon because of its low cost and availability. The source and drain are in direct contact with the top of the silicon and the gate is above a layer of oxide. When a positive voltage is applied to the gate, electrons are attracted to the substrate surface. This process opens a conducting channel from the source to the drain to complete the circuit. A transistor is used as a switch by opening and closing this circuit. The potential advantages to using SrTiO<sub>3</sub> as a

substrate are its superconducting properties and its easy integration with manganites and cuprates (4).

In recent years, significant research has been done in the field of oxide-electronics and in particular on SrTiO<sub>3</sub>. Work pertinent to our research was done by Ueno *et al.* that detailed a successful fabrication of an integrated circuit using SrTiO<sub>3</sub> as the substrate, aluminum for the contacts, and Al<sub>2</sub>O<sub>3</sub> for the insulator in his MISFET (5). We intended to reproduce Ueno's results in the first part of our project. In the second part of our project, we intended to expand upon Ueno's work by using doped SrTiO to modulate the transition temperature of the superconductivity.

The MISFET for our project was designed to induce a change in the superconducting temperature of the transistor, made possible since doped super-cooled SrTiO<sub>3</sub> acquires the property of superconductivity. Theoretically, varying the gate voltage of a MISFET would raise or lower the superconducting temperature. This effect creates a potentially invaluable component in microelectronic fabrication of superconducting devices (1).

SrTiO<sub>3</sub> has a perovskite structure that allows for the easy growth of manganites and cuprates. Manganites and cuprates are valuable in oxide-electronics as switching devices due to their unique electronic characteristics. Manganites with perovskite structure exhibit colossal magnetoresistance, a property enabling some materials to dramatically change their electrical resistance in the presence of a magnetic field. This resistance can be changed by several orders of magnitude (1). This property of manganites can also be exploited in metal-insulator-semiconductor switching devices like MISFETs (2). Cuprates are cheap high-temperature superconductors and are of great interest in the field of oxide-electronics. Both manganites and cuprates bond well with SrTiO<sub>3</sub> (2). With all the undiscovered potential of these versatile materials, it is important to research the capabilities of SrTiO<sub>3</sub>.

## **Fabricating and Testing of MISFET Prototypes and Results**

### ***Al<sub>2</sub>O<sub>3</sub> Sputtering Procedure for all Prototypes***

To clean the substrates, we filled two small beakers with acetone and placed a 6.35 mm x 6.35 mm x 0.5 mm silicon substrate and a matching insulator mask in one beaker and the sample holder in the other. We sonicated for ten minutes in acetone and repeated the same process with isopropanol.

To load the silicon sample and mask into the sputtering apparatus, we removed the metal shaft from the chamber and covered the orifice with aluminum foil to prevent contamination. We loaded the substrate and mask into the sample holder, securing them with clips and then wiped the shaft with isopropanol. We inserted the shaft into the orifice of the sputtering chamber to a depth of 10.16 cm and sealed it with Teflon tape. We opened the water-cooling valves to the turbomolecular pump and connected a Baratron gauge, which measured pressure. We turned on the mechanical pump, and once the Baratron read below 1.000 volt, we turned on the turbo pump. Once the turbo pump was at full power, we turned on the ion gauge and pumped the chamber down to better than  $5.0 \times 10^{-6}$  Torr.

For pre-sputtering, we connected water-cooling to the sample holder and the sputtering gun. We raised the pressure to 5 mTorr, using continuously flowing argon gas and, using oxygen

gas, raised the pressure another 0.5 mTorr. We raised the plasma power supply to 40 watts then increased it by 10 watts every two minutes to minimize the amount of power that was reflected back from the chamber. Pre-sputtering was done for 30 minutes.

For sputtering, we turned off the oxygen flow and waited five minutes. Then, we opened the shutter and sputtered at a rate of 20 Å/minute to a thickness of 1000 Å. When sputtering was complete, we closed the shutter, turned off the power, and shut off the argon flow. After venting the chamber with nitrogen, we removed the metal shaft and unloaded the substrate and mask.

### ***Fabrication Procedure for Silicon MISFET Prototype***

Our first MISFET prototype used silicon to become familiar with the fabrication process before using SrTiO<sub>3</sub>, since prototypes using silicon are known to work. To fabricate a silicon MISFET it was necessary to carry out four depositions: thick insulator, source and drain, gate dielectric, and gate. We used the appropriate nickel mask for each deposition. (Nickel masks can be obtained through various manufacturers or by cutting them using a machine located at most research institutions.) We first sputtered a 1000-Å thick insulator layer of Al<sub>2</sub>O<sub>3</sub> everywhere but on the masked region (active region) of the substrate. On either side of the masked region, we evaporated 600-Å thick gold source and drain contacts, each with a channel extending into the active region. Over this channel, we sputtered a 500-Å thick Al<sub>2</sub>O<sub>3</sub> gate dielectric. Finally, we evaporated a 500-Å thick gold gate contact, completing the MISFET.

### ***Gold Evaporation Procedure for Silicon MISFET Prototype***

We evaporated with gold instead of the aluminum suggested by Ueno since gold creates a better contact with silicon (2). The first step in depositing gold involved removing the sample holder from the evaporation chamber and covering its orifice with aluminum foil to prevent contamination. We set the shutter to cover the sample but not the quartz-crystal monitor (QCM). We loaded the sputtered substrate and a source/drain mask and secured them with clips. Then, we returned the sample holder to the chamber, sealing it with a rubber gasket and bolting it down. We removed the tungsten boat from the evaporation chamber and checked to see if it was ready to evaporate. In the event the tungsten was broken, we loaded a new coil. Around the tungsten, we wrapped gold wire and inserted the tungsten boat into the evaporation chamber. Before pumping down the chamber, we ensured the QCM reading was not fluctuating. (A stable QCM frequency reading was slightly below 6 MHz.) In the event that the QCM was fluctuating, we replaced the crystal in the QCM with a new one. We turned on the mechanical pump and, when the Baratron pressure gauge read below 1.00 volt, we turned on the turbo-molecular pump. We then turned on the ion gauge and water-cooling systems and pumped down the evaporation chamber to better than  $5.0 \times 10^{-6}$  Torr.

To evaporate the gold, we connected AC power to the tungsten boat and attached a voltmeter. We set the QCM program for gold evaporation and started the QCM program on the computer. We turned on the AC power and increased the voltage to 4 volts. We then monitored the QCM program and adjusted the voltage to keep the rate between 1-3 Å/second until we had evaporated 600 Å of gold. Then we closed the shutter, vented the chamber with oxygen, and removed the substrate.

### ***Problems with the Silicon MISFET Prototype***

We were unable to characterize the electrical capabilities of our first prototype because of sonication. We felt cleanliness was key throughout the fabrication process, since dust particles could seriously alter the capabilities of the transistor. Also, we thought that since transitions from one apparatus to another could cause possible contamination, we sonicated after our first round of  $\text{Al}_2\text{O}_3$  deposition. We found that sonication dislodged some of the evaporated gold after we had evaporated the source and drain. For this reason, we sonicated only before sputtering for all other fabrications. To solve possible contamination problems, we stored the substrate in a clean container between protocols.

### ***Fabrication Procedure for $\text{SrTiO}_3$ Prototype***

We fabricated a second prototype MISFET using  $\text{SrTiO}_3$  in place of silicon as a substrate. We followed the silicon MISFET fabrication procedure with the following modifications. We changed the way we loaded the masks. For the first prototype, we had placed masks directly on top of the substrate. Due to the fragility of  $\text{SrTiO}_3$ , there was a danger of the mask scratching the substrate so we elevated the mask 0.5 mm above the substrate. (Elevating the mask any higher would have caused shadowing.) While we used gold for the point contacts (source, drain, and gate) in the initial silicon prototype, we substituted aluminum as suggested by Ueno (5). In the second prototype, because there was lower resistivity between aluminum and  $\text{SrTiO}_3$  than there was between gold and  $\text{SrTiO}_3$ .

### ***Problems with Aluminum Evaporation***

Evaporating aluminum presented our next problem. Because the coil on the tungsten boat broke during the first evaporation, we increased the radius of the coil on the tungsten boat to make it proportional with the larger radius of the aluminum wire. After replacing the tungsten boat, we pumped down the chamber again and attempted to evaporate the aluminum onto the substrate, but we were not able to achieve a significant deposition rate. After venting the chamber, we realized that the aluminum had melted and fallen out of the tungsten boat. We replaced the tungsten boat yet again, this time by wrapping the coil tightly around the aluminum. Once again, the aluminum melted and fell out of the tungsten boat. We tried evaporating the aluminum three more times using this method of tungsten coiling and varying the voltage. However, we were not successful in evaporating the aluminum.

### **Conclusions**

Our engineering goal was to fabricate a MISFET using a  $\text{SrTiO}_3$  substrate. The first problem we ran into was when we tried sonicating after each process. Since sonication dislodged gold from the substrate, we altered our procedure so that we only sonicated before sputtering, and then stored the substrate between depositions to keep it clean. The second difficulty we encountered was a faulty QCM crystal, which we were able to replace. The third problem

occurred because we elevated the mask above the substrate due to the fragility of the SrTiO<sub>3</sub>. This caused problems when evaporating aluminum onto the substrate. Finally, we increased the radius of the coil to match the radius of the aluminum wire we had substituted for the gold, but since the tungsten could not be coiled tightly enough, the aluminum melted out of the coil.

To successfully evaporate the aluminum, we needed a more tightly coiled tungsten wire that would not break, but would also hold the aluminum in place as it evaporated. Because of time constraints, we were unable to complete this fabrication. In future studies, by using a larger-diameter and more tightly coiled wire, a viable SrTiO<sub>3</sub> MISFET could possibly be fabricated.

Though we were unsuccessful, our efforts did not prove fruitless. Beyond mastering sputtering and evaporation procedures to the point where we could address problems as they arose, we made a significant discovery regarding the fabrication of a SrTiO<sub>3</sub> MISFET. We discovered that the evaporation protocol needed modification. We learned that in order to successfully deposit the aluminum, we would require a thicker wire tungsten boat to hold the aluminum in place.

Future research might reveal the possibility of using a MISFET such as the one we were designing to vary the superconductivity temperature of SrTiO<sub>3</sub> through a piezo electric effect. Such research would open the door for the use of SrTiO<sub>3</sub> MISFETs in manganite and cuprate microelectronic applications.

## Acknowledgements

First and foremost, we would like to thank Dr. Allen Goldman for his guidance throughout our project. We would also like to thank Dr. Anand Bhattacharya and Melissa Eblen for their assistance in showing us how to use the metal evaporator and sputtering apparatus. Next, we would like to thank Lois Fruen for her help with our paper and her excellent job of leading the research program. Lastly, we would like to thank Team Research for all of their help during this school year.

## Sources Cited

1. M. Eblen, personal communication, (2004 July 22).
2. A. Bhattacharya, personal communication, (2004 July 22).
3. M. Riordan, L. Hoddeson, *Crystal Fire* (W.W. Norton & Co., New York, 1997).
4. R. Warner, Jr., B. Grung, *MOSFET Theory and Design* (Oxford University Press, New York, 1999) ch. 1.
5. K. Ueno *et al.*, *Applied Physics Letters* **83**, 1755-1757 (2003).

## Bibliography

- A Pacelli, *Introduction to MOSFET operation*, (Department of Electrical and Computer Engineering, Stony Brook, ed.2, 2001) pp. 1-17.
- B. Majkusiak, et. al., *IEEE Transactions on Electron Devices*, "Semiconductor thickness and back-gate voltage effects on the gate tunnel current in the MOS/SOI system with an

ultrathin oxide,” 47 (2000) Available from Inspec <<http://www.engineeringvillage2.com>> Accessed 2004 May 18.

- C. Kittel, *Introduction to Solid State Physics*, (John Wiley & Sons, Inc., New York, ed.7, 1996).
- J. Kolodzey, et. al., *IEEE Transactions on Electron Devices*, “Electrical conduction and dielectric breakdown in aluminum oxide insulators on silicon,” 47 (2000) Available from Inspec <<http://www.engineeringvillage2.com>> Accessed 2004 May 18.
- J. Shenoy, et. al., *Journal of Electronic Materials*, “Characterization and optimization of the SiO<sub>2</sub>/SiC metal-oxide semiconductor interface,” 24 (1995) Available from Inspec <<http://www.engineeringvillage2.com>> Accessed 2004 May 18.
- *Leybold Vacuum Products and Reference Book*, W. Umrath, Ed. (Leybold Vakuum GmbH, Germany, 2003) pp. D00.01-D00.138.
- M Andersson, et. al., *Physical Review B (Condensed Matter)*, “Surface-potential dependence of interface-state passivation in metal-tunnel-oxide-silicon diodes,” 50 (1994) Available from Inspec <<http://www.engineeringvillage2.com>> Accessed 2004 May 18.
- M. Riordan, L. Hoddeson, *Crystal Fire* (W.W. Norton & Co., New York, 1997).
- P. Lundgren, *Journal of Applied Physics*, “Impact of the gate material on the interface state density of metal-oxide-silicon devices with an ultrathin oxide layer,” 85 (1999) Available from Inspec <<http://www.engineeringvillage2.com>> Accessed 2004 May 18.
- R. Warner, Jr., B Grung, *MOSFET Theory and Design* (Oxford University Press, New York, 1999) ch. 1.
- S. Campbell, *The Science and Engineering of Microelectronic Fabrication*, (Oxford University Press, New York, 1996).
- Y. Ogita, et. al., *Thin Solid Films*, “Al<sub>2</sub>O<sub>3</sub> formation on Si by catalytic chemical vapor deposition,” 430 (2003) Available

## Appendix: Glossary

Drain: One of the point contacts to the MISFET.

Gate: The contact to which voltage is applied, inducing an inverse piezo electric effect in the substrate of the MISFET.

Gate Dielectric: The insulator layer of the MISFET.

MISFET: Metal-Insulator-Semiconductor Field-Effect transistor.

Sonication: The use of sound-wave energy to clean a substrate, mask, etc.

Source: One of the point contacts to the MISFET.

SrTiO<sub>3</sub>: Strontium titanate. The substrate used in our MISFET.

Substrate: The bulk of the MISFET, on top of which the source, drain, gate, and gate dielectric are deposited.

QCM: Quartz Crystal Monitor. Determines thickness of depositions through the vibration frequency of a crystal.